In the Claims

Claims 1-73 are canceled.

74. [Currently Amended] A field effect transistor fabrication method comprising:

providing semiconductive material including a channel region;

providing a source semiconductive region and a drain semiconductive region adjacent to the channel region of the semiconductive material, and wherein the providing the drain semiconductive region comprises providing at least one emitter;

providing gate dielectric material over the channel region; ~~and~~

providing a gate over the gate dielectric material and the channel region<u>; and</u>

<u>wherein the providing the drain semiconductive region and the providing the at least one emitter comprise forming the drain semiconductive region and the at least one emitter to comprise a monolithic semiconductive material</u>.

75. [Previously Presented] The method of claim 74 wherein the providing the semiconductive material comprises providing a thin film semiconductive layer.

76. [Previously Presented] The method of claim 74 wherein the providing the gate comprises polishing the gate dielectric material and gate material to form the gate aligned with the channel region of the semiconductive material.

77. [Previously Presented] The method of claim 74 wherein the providing the at least one emitter comprises providing a plurality of emitters.

78. [Previously Presented] The method of claim 74 wherein the providing the gate comprises providing the gate about the emitter.

79. [Previously Presented] A field effect transistor fabrication method comprising:

providing semiconductive material including a channel region;

providing a plurality of semiconductive regions adjacent to the channel region of the semiconductive material; and

self-aligning a gate with the semiconductive regions after the providing the semiconductive regions.

80. [Previously Presented] The method of claim 79 wherein the providing the semiconductive material comprises providing a thin film semiconductive layer.

81. [Previously Presented] The method of claim 79 further comprising:

providing gate dielectric material over the channel region; and

providing gate material over the gate dielectric material;

wherein the self-aligning comprises polishing the gate dielectric material and the gate material.

82. [Previously Presented] The method of claim 79 further comprising providing gate dielectric material over the channel region and the gate dielectric material including an upper surface substantially elevationally coincident with an upper surface of the gate.

83. [Currently Amended] A field emission device fabrication method comprising:

providing semiconductive material;

providing a plurality of semiconductive regions adjacent to the semiconductive material, and wherein the providing the semiconductive regions comprises providing one of the semiconductive regions comprising ~~an emitter~~ a plurality of emitters; and

providing a gate intermediate the semiconductive regions.

84. [Previously Presented] The method of claim 83 wherein the providing the semiconductive material comprises providing a thin film semiconductive layer.

85. [Previously Presented] The method of claim 83 wherein the providing the semiconductive regions and the providing the gate comprise forming a field effect transistor.

86. [Currently Amended] The method of claim 83 wherein the providing one of the semiconductive regions comprising ~~an emitter~~ the emitters comprises forming a tip of one of the ~~emitter~~ emitters elevationally below an upper surface of the gate and an upper surface of another one of the semiconductive regions.

87. Cancel.

88. [Currently Amended] The method of claim 83 wherein the providing the gate comprises providing the gate about one of the ~~emitter~~ emitters.

89. [Currently Amended] A field emission device operational method comprising:

providing a plurality of semiconductive regions adjacent to a channel region, and wherein at least one of the semiconductive regions comprises an emitter; ~~and~~

controlling current flow intermediate the semiconductive regions within the channel region and controlling emission of electrons from the field emitter using a gate intermediate the semiconductive regions; and

wherein the providing the at least one of the semiconductive regions comprising an emitter comprises etching to form the at least one semiconductive region and the emitter.

90. [Previously Presented] The method of claim 89 wherein the providing the semiconductive regions comprises providing the semiconductive regions adjacent to semiconductive material comprising a semiconductive layer.

91. [Previously Presented] The method of claim 89 wherein the providing the semiconductive regions comprises providing the semiconductive regions adjacent to semiconductive material comprising a thin film semiconductive layer.

92. [Previously Presented] The method of claim 89 further comprising configuring the gate and the semiconductive regions to form a field effect transistor.

93. [Previously Presented] A field effect transistor fabrication method comprising:

providing spaced semiconductive regions;

providing a channel region within semiconductive material between the spaced semiconductive regions;

providing gate dielectric material over the channel region; and

providing a gate intermediate the semiconductive regions and over the channel region;

wherein the gate dielectric layer has an upper surface elevationally coincident with an upper surface of the gate.

94. [Previously Presented] The method of claim 93 further comprising providing the semiconductive material comprising a thin film conductive layer.

95. [Previously Presented] The method of claim 93 wherein the semiconductive regions comprise an upper surface substantially elevationally coincident with an upper surface of the gate.

96. [Previously Presented] The method of claim 93 wherein the providing the gate comprises polishing gate material and the gate dielectric material.

Cancel claims 97-101.

102. [Previously Presented] A field effect transistor fabrication method comprising:

providing semiconductive material including a channel region;

providing a plurality of semiconductive regions adjacent to the channel region of the semiconductive material; and

providing a gate comprising gate material over the channel region of the semiconductive material without the use of a mask over the gate material.

103. [Previously Presented] The method of claim 102 wherein the providing the semiconductive material comprises providing a thin film semiconductive layer.

104. [Previously Presented] The method of claim 102 further comprising providing gate dielectric material over the semiconductive material, and wherein the providing the

gate comprises aligning the gate with the channel region of the semiconductive material using gate dielectric material.

105. [Previously Presented] The method of claim 102 wherein the providing the gate comprises removing portions of the gate material to self-align the gate with the channel region of the semiconductive material.

106. [Previously Presented] The method of claim 102 further comprising providing gate dielectric material over the semiconductive material, and wherein an upper surface of the gate dielectric material is substantially elevationally coincident with an upper surface of the gate.

107. [Previously Presented] The method of claim 102 wherein the providing the semiconductive regions comprises providing a drain region comprising a field emitter.

108. [Previously Presented] A field effect transistor fabrication method comprising:

providing spaced semiconductive regions including a channel region positioned therebetween;

providing gate material and gate dielectric material over the channel region; and

polishing the gate dielectric material and the gate material to form a gate intermediate the spaced semiconductive regions over the channel region.

109. [Previously Presented] The method of claim 108 wherein the polishing aligns the gate with the channel region.

110. [Previously Presented] The method of claim 108 wherein the providing the semiconductive regions comprises providing a drain comprising a field emitter.

111. [Previously Presented] The method of claim 108 wherein the polishing comprises chemical-mechanical polishing.

112. Cancel.

113. [Previously Presented] The method of claim 74 wherein the providing the drain semiconductive region and the providing the at least one emitter comprise etching.

114. [Currently Amended] The method of claim 83 wherein the providing the one of the semiconductive regions comprising ~~an emitter~~ <u>the emitters</u> comprises etching.

115. Cancel.

116. [New] A field effect transistor fabrication method comprising:

providing semiconductive material including a channel region;

providing a source semiconductive region and a drain semiconductive region adjacent to the channel region of the semiconductive material, and wherein the providing the drain semiconductive region comprises providing at least one emitter;

providing gate dielectric material over the channel region;

providing a gate over the gate dielectric material and the channel region; and

wherein the providing the at least one emitter comprises providing a plurality of emitters.

117. [New] A field effect transistor fabrication method comprising:

providing semiconductive material including a channel region;

providing a source semiconductive region and a drain semiconductive region adjacent to the channel region of the semiconductive material, and wherein the providing the drain semiconductive region comprises providing at least one emitter;

providing gate dielectric material over the channel region;

providing a gate over the gate dielectric material and the channel region; and

wherein the providing the drain semiconductive region and the providing the at least one emitter comprise etching.

118. [New] A field emission device fabrication method comprising:

providing semiconductive material;

providing a plurality of semiconductive regions adjacent to the semiconductive material, and wherein the providing the semiconductive regions comprises providing one of the semiconductive regions comprising an emitter;

providing a gate intermediate the semiconductive regions; and

wherein the providing one of the semiconductive regions comprising the emitter comprises forming a tip of the emitter elevationally below an upper surface of the gate and an upper surface of another one of the semiconductive regions.

119. [New] A field emission device fabrication method comprising:

providing semiconductive material;

providing a plurality of semiconductive regions adjacent to the semiconductive material, and wherein the providing the semiconductive regions comprises providing one of the semiconductive regions comprising an emitter;

providing a gate intermediate the semiconductive regions; and

wherein the providing the one of the semiconductive regions comprising the emitter comprises etching.